REMARKS

Claims 15, 17 and 19 remain for reconsideration. Claims 1-14, 18 and 20-24 were previously cancelled. Claim 16 is herein cancelled and the features therein incorporated into its parent claim 15.

The amendments introduced herein are believed proper under 37 C.F.R. § 1.116 as they do not introduce any new features which would require a further search and are believed to put the claims in condition for allowance or in better form for appeal. As such, entry of the amendment is respectfully solicited.

Applicants note with appreciation the Examiner's withdrawal of all previous rejections. All new art is relied upon in the Final Office Action as follows:

1. Claims 15-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over USP 7,088,322 to Koyama in view of USP 7,053,973 to Yamazaki; and

2. Claim 19 stands rejected under § 103(a) as being unpatentable over Koyama and Yamazaki further in view of USP 5,907,314 to Negishi.

These rejections are respectfully traversed based on the following discussion.

Briefly, embodiments are directed to increasing the functionality of an

LOCOS imaging device. As shown for example in Applicant's so-called AAPA of Figures 1 and 2, a pixel array comprising pixels 14 and a liquid crystal material may be sealed between an Si substrate 11 and a glass plate 12 by an adhesive strip 16. Active circuitry, such as for, example, driver and memory circuits 18 may be located separately on the same chip. This arrangement wastes valuable chip real estate.

In making the new rejections, the Examiner relies on Koyama for primarily teaching the claimed invention, but has additionally relied on Yamazaki for teaching the "adhesive strip" feature that Applicants introduced into the independent claim in the previous Amendment.

According independent claim 15 as now amended, "at least a portion of the frame buffer block includes memory cells co-located with pixel-elements of the pixel array". This is shown in Applicants Figures 3 and 4 where the frame buffers FBB1 and FBB2 (Figure 4) are located in the same space as the pixel array 33 (Figure 3).

The Examiner has relied on Koyama's Figure 20, element 2009, for teaching this feature. However, Figure 20 merely shows a "memory portion" 2009 connected to a pixel array 2007. The Figure does not show these components co-located occupying the same space as now claimed. To the contrary, they are shown as being clearly located in different spaces adjacent to one another. This arrangement does not lend itself to the valuable space savings advantage that Applicants realize by co-location.

This architecture provides advantages as explained in paragraph [0028]

wherein it states "*some embodiments of the invention include portions of the first and second frame buffers (FBB1 45 and FBB2 49), the associated first and second interface blocks (ICB1 46 and ICB2 48) and the control block (CB 43) located on the periphery of the die 40 and at least partially located within the area under an adhesive strip 41 that attaches the cover glass to the die 40, thus saving valuable die size. If the size and complexity of the device permits, it is preferable that the frame buffers are located completely within the area under the adhesive strip 41, thus providing increased functionality with no increase in die size*" (emphasis added).

This feature now recited in claim 15 also does not appear to be taught or suggested by either Yamazaki or Negishi; thus, the combination of these even with Koyama fails to establish prima facie obviousness under Section 103, and the rejection should be withdrawn.

The above features recited in the claims are not taught or suggested by the prior art of record. As such, it is respectfully requested that the outstanding rejections be withdrawn.

In view of the foregoing, it requested that the application be reconsidered, that claims 15, 17 and 19 be allowed and that the application be passed to issue. Please charge any shortages and credit any overcharges to Intel's Deposit Account number 50-0221.

Respectfully submitted,

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